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High-Speed ADC Sets Input Common-Mode Range

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Differential, DC-coupled connections to a high-speed ADC are typically found in radio receivers with direct down-conversion. Such circuits have a Zero-IF (ZIF) architecture that features an RF quadrature demodulator and dual baseband ADC. ZIF circuits are popular because they eliminate multiple IF down-conversions and SAW filters. DC-coupled connections are desirable in a ZIF architecture for several reasons: they accept in-phase (I) and quadrature (Q) baseband data with an information bandwidth extending close to dc, they eliminate bulky coupling capacitors between the RF down-converter and high-speed ADC, and they eliminate power-sequencing delays caused by the coupling capacitor's discharge time.

The importance of Vcm for the ADC is apparent when you consider the following:

- With variation in the supply voltage (VDD), signals sourced by the RF quadrature demodulator present a wide range of common-mode voltages to the ADC.
- Input common-mode levels extending beyond the ADC's Vcm range generate harmonic distortion that reduces the dynamic range. A proper Vcm dc bias therefore optimizes the amplifier and ADC linearity, minimizing distortion and improving the bit-error rate (BER).

In Figure 1, UI helps to simplify the dc-coupled, differential analog interface between RF front-end, drive amplifier, and ADC. The circuit, comprising a dual 8-bit 40Msps ADC (U1) and two quad single-supply wideband amplifiers (U2-U3), accommodates a wide range of input common-

mode voltages at the analog interface between the RF quadrature demodulator (a differential, dc-coupled signal source) and high-speed ADC. The ADC provides sufficient Signal to Noise Plus Distortion (SINAD) and Spurious-Free Dynamic Range (SFDR) to demodulate a 3.84MHz wideband QPSK communication link. You should select U2 and U3 for adequate SFDR and input common-mode range. U1 draws 90mW from a single 3V supply.

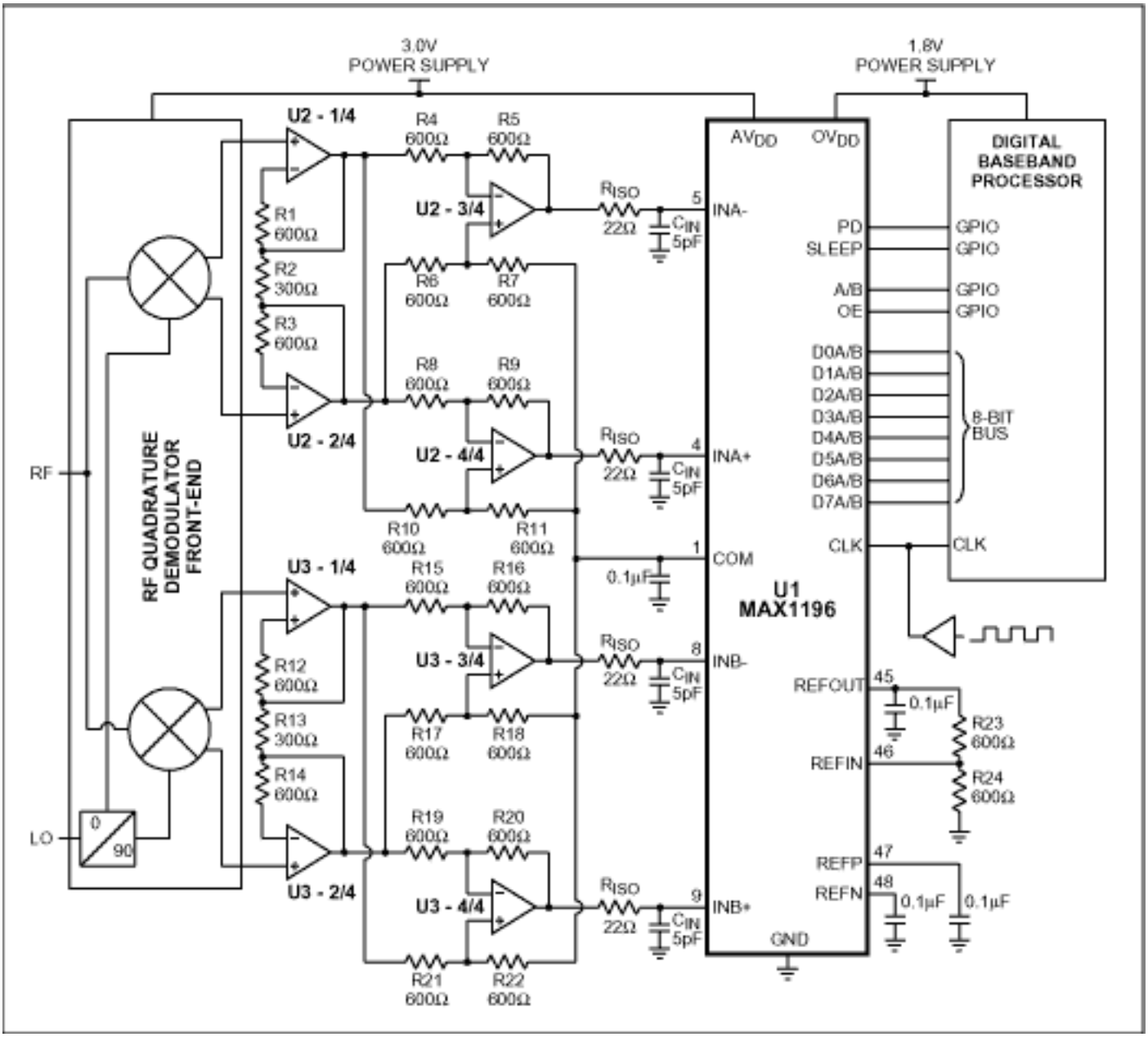

Figure 1. This high-speed ADC (U1) uses its COM output to set a precise common-mode level.

Simplifying the translation of Vcm are U1's dc common mode output (COM, pin 1), REFIN (pin 46), and REFOUT (pin 45). COM provides a dc output (VDD/2) that matches the input common-mode range of U1 despite VDD variations. REFIN and REFOUT set the ADC full-scale range via resistor divider R23-R24, thereby optimizing the input amplifier SFDR and ADC dynamic range.

U2 and U3 are configured for dc-coupled differential inputs and outputs, with 15dB gain, which provides the ADC with a full-scale (FS) input of $1V_{p-p}$. To preserve the receiver's dynamic range,

choose U2/U3 amplifiers that specify an SFDR 10dB better than the ADC's 48.7dB SINAD. U1's FS voltage is set by R23 and R24:

FS = R24/(R23+R24) x REFOUT. (REFOUT = 2.048V)

The COM voltage (pin 1 of U1) equals Vdd/2, or 1.5V when VDD = 3V. This voltage also equals the input Vcm range of U1. Thus, as VDD changes with temperature and supply-voltage tolerance, COM and Vcm track each other to ensure a proper matching of dc voltage levels. The COM pin sources 5mA, and can be used as needed to set the dc level of other circuit elements in the system. Because the COM internal buffers are powered down during ADC shutdown, this level-setting approach saves more power than does a continuously on, 2-resistor voltage divider.

A typical application for the Figure 1 circuit is a WCDMA receiver, for which the input signal to each ADC channel is one-half the 3.84Mcps chip rate. Two benefits follow when the signal is over-sampled by U1 at four times the chip rate (Fclk = 15.36MHz). First, oversampling eases the design of an anti-alias filter by pushing the image beyond two octaves, to 13.44MHz and 17.28MHz (FI = Fs ± Fa). Second, oversampling yields a processing gain of 6dB: SNR = 10log(Fs/2BW).

UI's digital outputs are supplied by 0VDD = +1.8V, which helps to minimize power consumption. The +1.8V bus lowers digital signal swings, which reduces power according to the relation $P = CV^2F$ (once for each line of the 8-bit buss). UI's digital outputs are multiplexed, which allows the dual 8-bit ADC to interface via a single 8-bit bus. The multiplex feature also helps to minimize the digital I/O pin count, save board space, reduce digital ASIC costs, and improve system reliability.

Other options: The MAX1185 is a dual 10-bit ADC, pin-compatible with the MAX1196. Both parts are packaged in a 7x7mm 48-pin TQFP package with exposed paddle. The MAX1192 is an ultra-low-power, miniature dual 8-bit ADC that consumes less than 25mW at 3V. It comes in a 5x5mm, 28-pin Thin QFN package.

More Information

MAX1185: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX1192: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX1196: QuickView -- Full (PDF) Data Sheet -- Free Samples